	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L14	2	10/731,191	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:30
2	BRS	L15	0	("2005/0144508").URPN.	USPAT	2006/06/25 15:33
3	BRS	L16	38	((servic$4 or defect$4 or problem or technical or state or status) with (memory or storage or ram) with (remov$4 or portabl$4 or detach$4)).ti.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:42
4	BRS	L17	1983	((servic$4 or defect$4 or problem or technical or state or status) with (memory or storage or ram) with (remov$4 or portabl$4 or detach$4)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:43

	Type	L #	Hits	Search Text	DBs	Time Stamp
5	BRS	L18	3720	(711/115 or 239/492 or 714/1,25,42).ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:48
6	BRS	L19	1323	(711/115 or 239/492 or 714/1 or 711/25 or 711/42).ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:49
7	BRS	L20	3720	(711/115 or 239/492 or 714/1 or 714/25 or 714/42).ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:49
8	BRS	L21	56	17 and 20	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	2006/06/25 15:49

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CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Patent No. 60/408,205, filed on Sep. 5, 2002, entitled "Functional Interrupt Mitigation for Fault Tolerant Computer," naming David Czajkowski as first named inventor and Darrell Sellers as second named inventor, of which is hereby incorporated by reference in its entirety.

---------- KWIC ---------

Current US Classification, US Primary Class/Subclass - CCPR (1):
714/25

Claims Text - CLTX (3):
2. A system of claim 1 further comprising a microprocessor software routine configured to send maintenance data to microprocessor memory prior to functional interrupt and configured to read said maintenance data from

microprocessor memory after microprocessor's removal from functionally interrupted state and use maintenance data to restart microprocessor's application software routines.

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(54) FUNCTIONAL INTERRUPT MITIGATION FOR FAULT TOLERANT COMPUTER

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(52) U.S. Cl. 714/25

(57) ABSTRACT

A new method for the detection and correction of environmentally induced functional interrupts (or "hangs") induced in computers or microprocessors caused by external sources of single event upsets (SEU) which propagate into the internal control functions, or circuits, of the microprocessor. This method is named Hardened Core (or H-Core) and is based upon the addition of an environmentally hardened circuit added into the computer system and connected to the microprocessor to provide monitoring and interrupt or reset to the microprocessor when a functional interrupt occurs. The Hardened Core method can be combined with another method for the detection and correction of single bit errors or faults induced in a computer or microprocessor caused by external sources SEUs. This method is named Time-Triple Modular Redundancy (TTMR) and is based upon the idea that very long instruction word (VLIW) style microprocessors provide externally controllable parallel computing elements which can be used to combine time redundant and spatially redundant fault error detection and correction techniques. This method is completed in a single microprocessor, which substitute for the traditional multi-processor redundancy techniques, such as Triple Modular Redundancy (TMR).